A Compact CPW-Based Single-Layer Injection-Locked Active Antenna for Array Applications

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***Abstract*—A compact single-layer coplanar waveguide (CPW)-fed active patch antenna oscillator at 9.81 GHz is presented based on a commercially available GaAs FET, which is centered behind the patch for tight packing. The positive feedback for the oscillation is accomplished through twin-slot aperture coupling to the patch. This results in a design having its longest dimension equal to 26.6 mm at 9.81 GHz. A low-power injection signal is applied to stabilize the oscillation through parasitic coupling at the CPW side of the circuit. This parasitic coupling is achieved by electromagnetic coupling of the locking signal to the gate of the FET. The measured effective isotropic radiated power is 19.6 dBm, whereas the worse-case front-to-back ratio is about 15 dB with the cross-polarized fields better than −20 dB at broadside. The measured phase noise of the unlocked and locked signals are −63.28 and −107.5 dBc/Hz, respectively, at a 100-kHz offset away from the carrier. This compact design is ideally suited as a unit cell in injection-locked phased-array architectures.**

***Index Terms*—Active antennas, CPW, injection locking, patch antennas, phased arrays.**

I. Introduction

In THE pioneering work by Liao and York, it was demonstrated that an externally injection-locked active-antenna array is capable of electronic scanning through detuning without the use of phase shifters [1]. Depending on the choice of the feeding network and the inter-element spacing, various maximum beam-steering angles ranging from 21° to 70° can be achieved [1]–[5]. In general, these types of novel phased-array designs require a compact active antenna as a unit element (to avoid grating lobes when scanning) and a proper network for feeding the injection-locking control signal for a practical and simple structure, with reduced spurious radiation and minimum number of components.

Most of the reported injection-locked phased-array designs utilize patch antennas for implementing the unit-cell elements [1]–[5]. This is due to the well-established virtues of patch antennas such as that they are low cost, highly integrable with monolithic-microwave integrated-circuit (MMIC) circuitry, and are good resonators for self-oscillating active-antenna designs. In order to fully utilize the inherent advantages of patch antennas, several design issues need to be considered, such as spurious feed radiation, surface-wave leakage, and a requirement for a compact and simple active unit cell. To resolve these issues, a single-layer coplanar waveguide (CPW)-based active patch antenna unit cell was developed by these authors and is presented in [6]. The main advantages of the structure in [6] are that no via-holes are necessary for grounding, only a single layer is required, and that electromagnetic coupling of the patch is used for closing the feedback loop, which further reduces the complexity of the antenna structure. These benefits do not compromise the quality of the performance when compared to aperture coupled designs [7], [8], making the design of [6] suitable for low-cost proximity sensing and collision avoidance applications. However, the previous design reported in [6] required a long delay line for adjusting the phase of the feedback loop, thus forcing the device to be placed outside of the patch. In addition, that structure did not feature injection-locking capabilities. Both of these deficiencies make the design of [6] less suitable for array implementations.

In this paper, a significantly improved design compared to [6] and an associated design methodology are presented. In this improved version, the active element (GaAs FET) is centered behind the patch antenna. In particular, the GaAs FET is embedded in a CPW-fed twin-slot arrangement, which is electromagnetically coupled to a patch antenna resonator. Two open-circuited CPW stubs are utilized for gate and drain matching. This proposed approach inherits the advantages from the previous design [6], with the added benefit of a compact size. In addition, a low-power injection signal serves to stabilize the oscillation through parasitic coupling to the gate of the FET at the CPW side of the circuit, thereby avoiding the need of using microstrip couplers at the patch side [5]; this leads to lower parasitic and cross-polarized radiation.

The structure of this paper is as follows. In Section II, the configuration and design methodology of the improved active-antenna element are presented, followed by the design of the injection-locking feed network. Section III describes the experimental procedure and the results obtained for the active antenna, including the radiation patterns when the active element is locked at 9.81 GHz, the phase-noise performance, the effective isotropic radiated power (EIRP), the dc-to-RF efficiency, and the locking range of the active antenna.

II. Active-Antenna Configuration and Design

A. Configuration

The active antenna proposed here is depicted in Fig. 1. As shown, the front side of the substrate hosts the patch,

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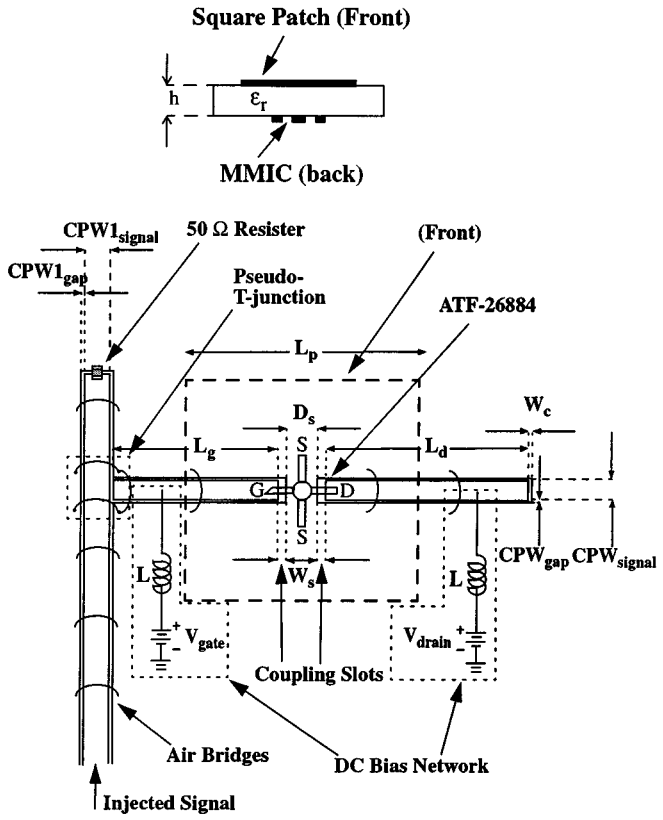

Fig. 1. Layout of the active antenna. $\varepsilon_r = 2.33$, $h = 1.57$ mm, $L_p = 9$ mm, $L_g = 9.5$ mm, $L_d = 13.6$ mm, $W_c = 0.2$ mm, $W_s = 0.4$ mm, $D_s = 2.3$ mm, $CPW_{\text{signal}} = 2.5$ mm, $CPW_{\text{gap}} = 0.1$ mm, $CPW1_{\text{signal}} = 3$ mm, $CPW1_{\text{gap}} = 0.2$ mm, $L = 5$ mH, $V_{\text{gate}} = -0.785$ V, and $V_{\text{drain}} = 3.5$ V.

whereas the active circuitry is accommodated at the back side in 50-Ω CPW technology. The substrate thickness is chosen to be 1.57 mm for a good compromise among surface-wave excitation, bandwidth, and front-to-back ratio. The injection locked active antenna is designed to operate at 9.81 GHz using an ATF-26884 GaAs FET from Hewlett-Packard as the active element. Compared with the design presented in [6], where the device was located outside of the patch, the new design centers the device in between the coupling slots and behind the patch for compactness. For matching, two open-circuited CPW stubs are used at the gate and drain of the FET, as shown in Fig. 1. For dc biasing, two discrete inductors with $L = 5$ mH soldered on the board with silver epoxy are utilized as RF chokes, as shown in Fig. 1. Furthermore, the injection-locking signal is fed on a 50-Ω terminated CPW transmission line, as also shown in Fig. 1. Parasitic coupling between the locking signal and active antenna is achieved by connecting the injection signal line to the open-circuited stub at the gate of the FET using a pseudo-T-junction (see Fig. 1). Coupling at the gate of the active antenna has the advantage of lower power leakage of the injection signal and, thus, lower parasitic radiation than when coupling to the drain. In addition, this approach avoids the use of microstrip coupling to the patch side for implementing the injection-locking feed network, in contrast to [5], which helps to maintain low cross-polarization and low parasitic radiation at broadside.

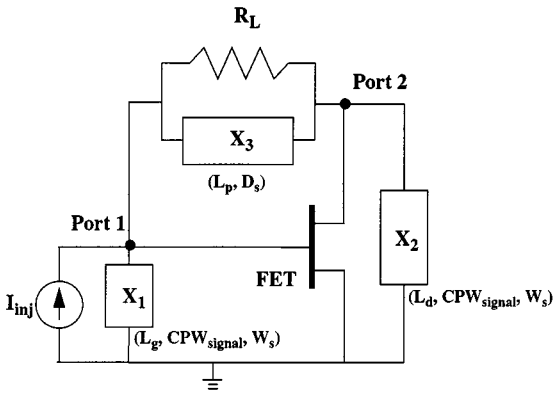

Fig. 2. Optimum 9.81-GHz oscillator circuit. $R_L = 32.3\ \Omega$, $X_1/\omega = 0.665$ nH, $X_2/\omega = 2.08$ nH, and $X_3/\omega = 0.628$ nH.

B. Design

Fig. 2 shows the shunt feedback equivalent circuit of the overall structure. The shunt embedding network for the FET is represented by a load resistance R_L, and three reactances X_1, X_2 and X_3. The current source I_{inj} represents the injection signal. The resistance R_L and the reactance X_3 model the radiation resistance and reactance of the patch antenna, respectively, whereas X_1 and X_2 represent the cumulative reactances of the capacitive coupling slots and the open-circuited CPW matching stubs. The physical dimensions of Fig. 1 affecting the elements of the equivalent circuit are marked in Fig. 2 for convenience.

The oscillator design follows the procedure outlined in [9]–[11] for calculating the shunt embedding network for the FET. The small-signal S-parameters of the FET are measured over a frequency range from 9–11 GHz using an HP8722C vector network analyzer and a custom-made thru-reflect line (TRL) calibration kit for the specific CPW environment. Reasonable values for the large-signal S-parameters can be estimated by appropriately modifying the magnitude of the small-signal S_{21} while keeping the remaining small-signal parameters the same [4], [9]. The estimated large-signal S_{21} is obtained as follows. First, using the small-signal parameters of the device, the corresponding small-signal gain G_0, can be calculated from the following equations [9]:

$$G_0 = \frac{\left|\frac{S_{21}}{S_{12}}\right|^2 - 1}{2\left\{K\left|\frac{S_{21}}{S_{12}}\right| - 1\right\}} \tag{1}$$

$$K = \frac{1 + |S_{11}S_{22} - S_{21}S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}|\,|S_{21}|} \tag{2}$$

where K is the Rollett stability factor. Next, the maximum efficient gain at the point of maximum oscillator power G_{ME} can be calculated using the following expression:

$$G_{\text{ME}}(\text{max. oscillator power}) = \frac{G_0 - 1}{\ln(G_0)}. \tag{3}$$

Equation (2) is derived in [9] using the approximated power-gain saturation characteristics of a FET power amplifier.

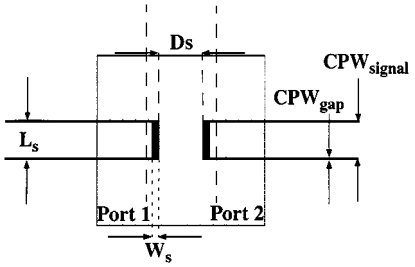

Fig. 3. Layout of the slot-coupled patch. $L_s = 2.7$ mm, $W_s = 0.4$ mm, $D_s = 2.3$ mm, $CPW_{\text{signal}} = 2.5$ mm, and $CPW_{\text{gap}} = 0.1$ mm.

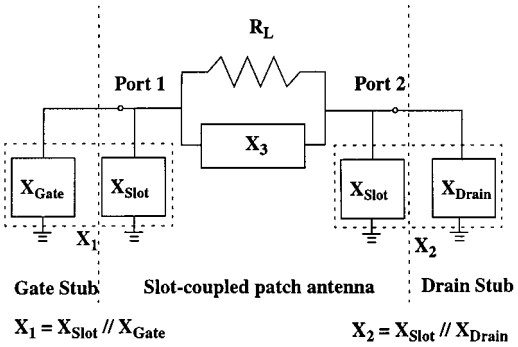

Fig. 4. Schematic for the final passive structure. $R_L = 43.6\ \Omega$, $X_3/\omega = 0.314$ pF, $X_{\text{Slot}}/\omega = 0.135$ pF, $X_{\text{Drain}}/\omega = 0.105$ pF, and $X_{\text{Gate}}/\omega = 0.895$ nH.

Once G_{ME} has been calculated, the large-signal $|S_{21}|$ can be obtained by substituting G_0 with G_{ME} into (1). In this design, the device has a small-signal $|S_{21}| = 7.8$ dB and a $G_0 = 11.1$ dB corresponding to a $G_{\text{ME}} = 6.7$ dB and yielding a large-signal $|S_{21}| = 3.6$ dB. With these large-signal S-parameter values, the shunt feedback embedding circuit, shown in Fig. 2, is calculated from a set of equations given in [11] for achieving an optimum oscillation condition at the design frequency of 9.81 GHz. With reference to Fig. 2, this procedure yields

$$R_L = 32.3\ \Omega \tag{4a}$$

$$X_1/\omega = 0.665\ \text{nH} \tag{4b}$$

$$X_2/\omega = 2.08\ \text{nH} \tag{4c}$$

$$X_3/\omega = 0.628\ \text{nH}. \tag{4d}$$

After calculating the embedding circuit from the measured S-parameters of the FET, a distributed version of the embedding circuit is realized by the slot-coupled patch and the two matching stubs at the gate and drain of the active device. The design of the slot-coupled patch is based on HP Momentum, a method-of-moments full-wave electromagnetic planar solver. A symmetric structure for the slot-coupled patch is adopted for a simple design and is shown in Fig. 3.

First, using HP Momentum, the dimension of the patch L_p (see Fig. 1) has been designed to achieve a condition close to antenna resonance at 9.81 GHz, and to yield a good front-to-back ratio [8], [12]. In addition, a fixed distance of $D_s = 2.3$ mm between the coupling slots was maintained for accommodating the FET symmetrically in the center of the active antenna (see Fig. 3). The S-parameters of the resulting structure were then

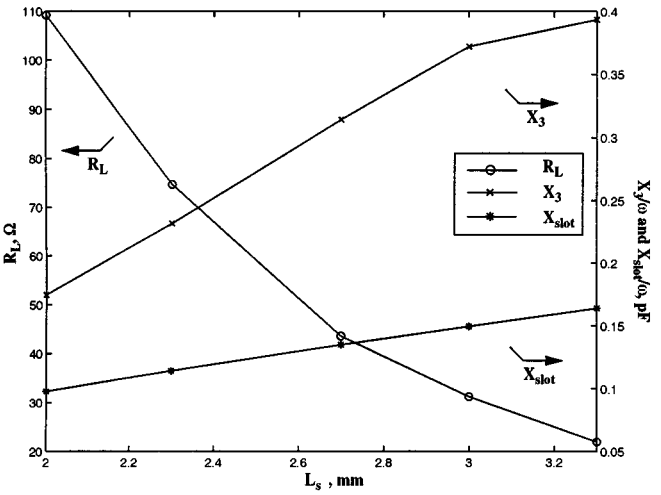

Fig. 5. R_L, X_3, and X_{Slot} for different slot lengths L_s.

translated into the equivalent circuit shown in Fig. 4, which consists of the complex shunt radiation impedance $R_L + jX_3$ and two shunt reactances X_{Slot} for representing the capacitance of the coupling slots. Subsequently, a parametric analysis relating the dimensions L_s, D_s, and W_s (see Fig. 3) with the equivalent circuit in Fig. 4 has been undertaken based on HP Momentum. It was found that the equivalent lumped elements R_L, X_3, and X_{Slot} are less sensitive to variations of dimensions D_s and W_s. On the other hand, there is greater sensitivity on the length of the coupling slots L_s (see Fig. 3). For this latter case, the variation of R_L, X_3, and X_{Slot} is shown as a function of L_s in Fig. 5. Based on Fig. 5, the length of the slots L_s is chosen such that the required embedding R_L value of (4a) is closely achieved. In this example, a value of $L_s = 2.7$ mm has been chosen, yielding an $R_L = 43.6\ \Omega$, which is close to the value of $R_L = 32.3\ \Omega$ required by (4a). It was not judged prudent to choose an even longer slot L_s to further reduce the patch resistance R_L in order to contain parasitic radiation from the slots and CPW lines, and to maintain the integrity of the CPW ground plane. Furthermore, it should be noted that increasing the patch dimension (L_p above resonance) would swing the patch reactance X_3 in Fig. 5 from capacitive to inductive as required by (4d), but at the expense of a longer patch and a lower front-to-back ratio. A size L_p of 9 mm is chosen for this compact design.

Subsequently, the lengths of the two open-ended CPW stubs, represented by X_{Gate} and X_{Drain} in Fig. 4, were optimized in order to meet the oscillation condition. Specifically, the length of the stubs are computed such that the reactances of the stubs X_{Gate} and X_{Drain}, plus the reactances of the coupling slots X_{slot} are equal to the calculated values X_1 and X_2 of the embedding network, i.e.,

$$X_1 = X_{\text{Slot}} // X_{\text{Gate}} \tag{5}$$

$$X_2 = X_{\text{Slot}} // X_{\text{Drain}}. \tag{6}$$

Based on this procedure, the minimum possible lengths for the gate and drain stubs have been determined to be 9.5 and 1.1 mm, respectively. However, a one-half guided wavelength line is added to the drain stub, resulting in a value of 13.6 mm. Adding this extra section to the drain stub avoids the unwanted

TABLE I
SUMMARY OF THE MEASURED CHARACTERISTICS OF THE ACTIVE ANTENNA

$V_{ds} = 3.5$V		min	max
Free Running Frequency	f_{osc}(GHz)	9.789	9.845
	V_{gs}(Volts)	-0.604	-1.024
	I_{gs}(mA)	32.5	23
Locking Range ($f_{free-running}$=9.81 GHz)			
P_{inj} = -10 dBm	f_{inj}(GHz)	9.805	9.815
P_{inj} = 0 dBm	f_{inj}(GHz)	9.795	9.826

coupling between the open-circuited stub and the patch antenna, at the expense of a larger active-antenna size. The overall structure is verified and fine tuned using the oscillation test in the schematic part of HP ADS, a popular microwave circuit simulator. Finally, the layout of the pseudo-T-junction (see Fig. 1) for the injection-locking network is simulated using HP Momentum, and a coupling level of -12 dB is obtained. Injection locking is applied at the gate stub of the FET via the pseudo-T-junction to minimize the power leakage and parasitic radiation from the injected signal through the active antenna. The layout of the injection-locking network is shown in Fig. 1. As shown, the injection line is terminated to a 50-Ω resistor to avoid standing waves along the line.

III. EXPERIMENTAL RESULTS

The active antenna is built on a Duroid 5870 substrate of $\varepsilon_r = 2.33$ with a thickness of $h = 1.57$ mm, as shown in Fig. 1. Air bridges are built on top of the CPW lines, especially around the pseudo-T-junction and the injection line, to suppress the parasitic slot-line mode. A free-running oscillation frequency of 9.817 GHz$\pm$28 MHz has been measured using an HP8563E spectrum analyzer. On the other hand, an HP83620B series swept signal generator is used to provide a low-noise injection signal to the active antenna. When the active antenna is locked to the injection signal, a locking range of 10 and 31 MHz is obtained for an injection power level of -10 and 0 dBm, respectively. The measured characteristics of the active antenna are summarized in Table I. The RF-spectrum of the free-running and locked signals with a 0 dBm of injected power as measured with the HP8563E spectrum analyzer are shown in Fig. 6. Using the same spectrum analyzer, the phase noise of the locked and unlocked signals is measured manually based on the following method. With the resolution bandwidth of the spectrum analyzer set to $\mathrm{RBW} = 1$ kHz, sideband power levels are measured and averaged at 100 kHz away from the carrier. The following relation then applies [13]:

$$P_{\text{noise}} = P_{\text{sideband}} - P_{\text{carrier}} - 10\log(\mathrm{RBW})\ \text{dB}. \quad (7)$$

Using this procedure, the phase noise of the locked and unlocked signal is calculated to be -107.5 and -63.28 dBc/Hz, respectively, both at a 100-kHz offset away from the carrier. Note that the phase-noise software utility for the HP8563E is not reliable when measuring the phase noise of an unlocked active antenna because it assumes that the frequency of the signal being examined does not drift in time, which is not the case for an unlocked active antenna. Clearly, a cleaner spectrum is observed when the active antenna is locked to a stable injection signal, which is consistent with phase-noise analysis of injection locking [14].

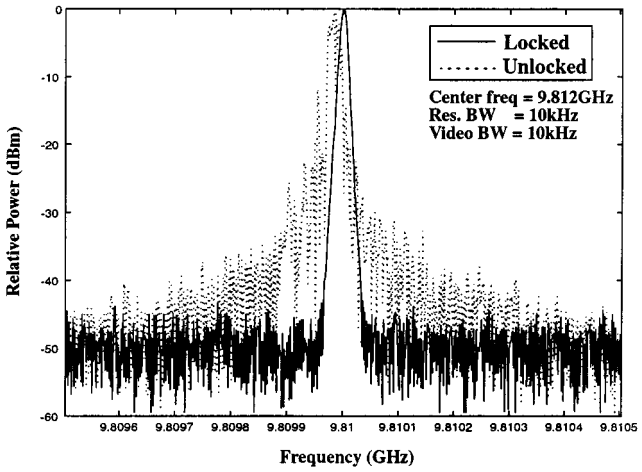

Fig. 6. Measured spectrum of the free-running and locked signal.

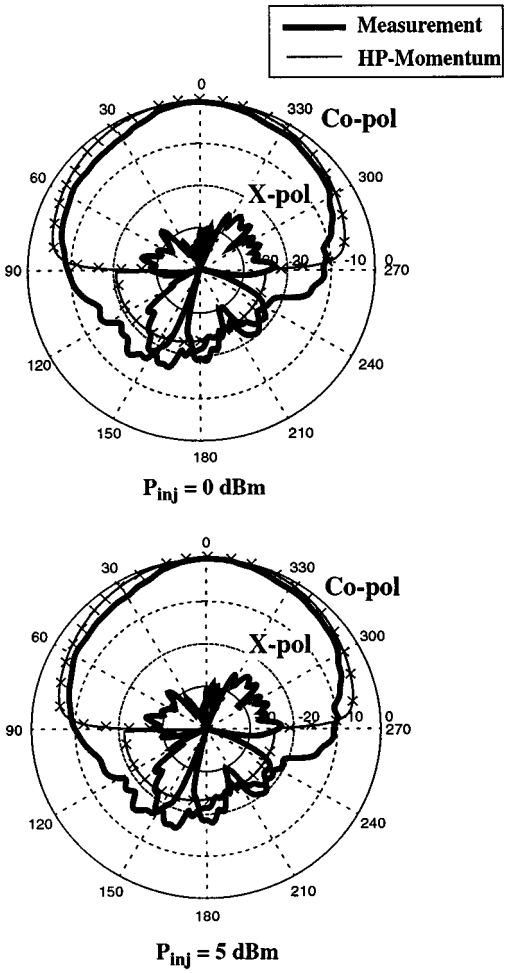

Fig. 7. Measured E-plane active radiation pattern at 9.81 GHz.

The active-antenna patterns of the unit cell when locked have been tested in the anechoic chamber of the University of Toronto, Toronto, ON, Canada. Figs. 7 and 8 show the

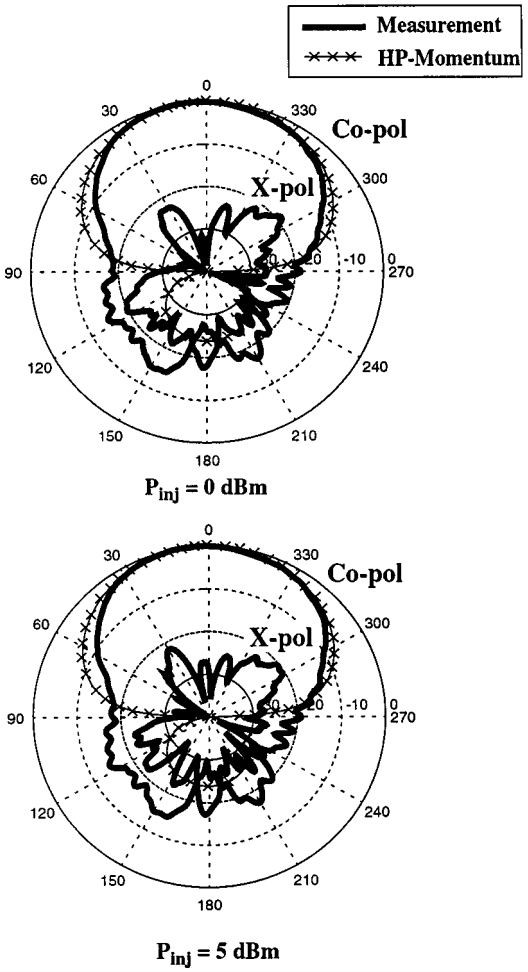

Fig. 8. Measured H-plane active radiation patterns at 9.81 GHz.

TABLE II
SUMMARY OF THE MEASURED PERFORMANCE OF THE ACTIVE ANTENNA

$V_{ds} = 3.5$V	
EIRP	19.6 dBm
P_{eff}	11.3 dBm
Directivity	8.3 dB
η_{dc-rf}	14 %

measured E- and H-plane radiation patterns at 9.81 GHz for injection signal levels of 0 and 5 dBm, together with the co-polarized patterns simulated using HP Momentum. As shown, the worse cross-polarization appears in the H-plane, but does not exceed the level of 15 dB. On the other hand, the measured front-to-back ratio has been found to be better than 15 dB. Both the measured cross-polarization levels and the front-to-back ratio compare favorably with those of the two-layer microstrip structures of [7] and [8], indicating no performance degradation of the proposed single-layer CPW approach. In addition, a close comparison of Figs. 7 and 8 indicates that the power of the injection signal does not affect the radiation patterns, suggesting a low parasitic radiation from the injection-locking network.

Finally, based on the method described in [7], the EIRP of the locked patterns at 9.81 GHz has been measured to be 19.6 dBm, at a dc-bias condition of $V_{\rm drain}$ and $I_{\rm drain}$ of 3.5 V and 28 mA, respectively. From the measured radiation patterns, the directivity of the antenna is estimated to be $D = 8.3$ dB, resulting in an effective transmitter power $P_{eff} = \text{EIRP} - D$, of 11.3 dBm and a dc-to-RF efficiency of 14%. These results are summarized in Table II. It should be noted that the presented unit cell has not been optimized for high dc-to-RF efficiency. This can be accomplished by operating the underlying amplifier in a class-E mode [15]. It should be pointed out that, due to the CPW slot coupling used at the center of the patch (see Fig. 3), the input embedding impedance presented to the device at the second harmonic closely corresponds to an open circuit. This assertion has been verified both using HP Momentum, as well as experimentally, and it is the primary requirement for class-E operation [16].

IV. SUMMARY AND CONCLUSION

A compact injection-locked single-layer active-antenna oscillator based on 50-Ω CPW technology has been successfully designed and tested at 9.81 GHz. This CPW-based design eliminates the use of via-holes, and tightly integrates the FET device with the patch antenna; thus making it suitable for injection-locked phased-array applications. By utilizing slot coupling from the device to the patch for closing the feedback loop, the number of lumped-element components is minimized, and the size of the unit cell, as well as parasitic radiation, are reduced. In addition, an injection-locking path is established at the CPW side through parasitic coupling to the gate of the FET, leading to low spurious leakage of the injected power.

Despite the tight packing of the device to the antenna, a modular design methodology has been presented, which allows the implementation of the proposed layout in a systematic way. The final measured results for the designed active antenna at 9.81 GHz demonstrate clean E- and H-plane patterns, exhibiting a cross-polarization level better than -15 dB. The active antenna achieves an EIRP of 19.6 dBm, a front-to-back ratio of 15 dB, and a locking range of 31 MHz. On the other hand, the measured phase noise of the locked signal is -107.5 dBc/Hz at a 100-kHz offset away from the carrier. This compact unit-cell design can be utilized as the building block in phase-shifterless beam-steering array applications.

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